AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-23 (Cancelled)

24. (New) An integrated circuit comprising:

a test controller;

a logic unit controller of the integrated circuit;

a single test bus of the integrated circuit, the single test bus coupled between the test controller and the logic unit controller;

a plurality of design for test features of the integrated circuit, the design for test features coupled to the logic unit controller; and

a logic unit of the integrated circuit, the logic unit coupled to the logic unit controller and to the design for test features,

wherein the test controller is to provide a global control signal as a packet including a plurality of different types of instruction signals to the logic unit controller over the single test bus, wherein the logic unit controller is to receive the packet and provide a plurality of different types of instruction signals to a design for test feature.

25. (New) The integrated circuit of claim 24, wherein the different types of instruction signals include a shift signal and a load signal.

26. (New) The integrated circuit of claim 24, wherein the test controller has an instruction register and a test access port finite state machine (TAP FSM), and wherein the test controller is to provide a subset of all states of the TAP FSM to the logic unit controller over the single test bus.

27. (New) The integrated circuit of claim 24, wherein the packet travels as a single speed critical global control signal, and wherein the plurality of different types of instruction signals provided to the design for test feature are not speed critical.

28. (New) The integrated circuit of claim 24, wherein the logic unit controller comprises a deskew controller.

29. (New) The integrated circuit of claim 24, wherein the packet is provided based at least in part on a clock other than a core clock of the integrated circuit.

30. (New) The integrated circuit of claim 24, wherein the single test bus comprises a plurality of lines that have a single routing path between the test controller and the logic unit controller.

31. (New) The integrated circuit of claim 24, wherein the single test bus comprises nineteen lines.

32. (New) The integrated circuit of claim 24, wherein the single test bus comprises n number of lines such that

$$n = a + \log_2 i$$

where a is the number of ancillary transmission bits, and where $\log_2 i$ is the number of instruction bits.

33. (New) The integrated circuit of claim 32, wherein the number of instruction bits are represented within the content of the instruction register, and wherein the instruction register is compliant with IEEE 1149.1.

34. (New) The integrated circuit of claim 32, wherein the ancillary transmission bits include at least one of a clock signal, at least one state of a test access port finite state machine, a security bit, a test data input, and a counter value.

35. (New) The integrated circuit of claim 34, wherein the at least one state of a test access port finite state machine is encoded in three bits.

36. (New) The integrated circuit of claim 34, wherein the at least one state of the test access port finite state machine is allocated into a one-bit test-logic-reset state, a one bit run-test/idle state, and a two-bit residual state.

37. (New) A platform comprising:

a support structure;

a processor, a memory controller, a memory chip, and a graphics controller each disposed on and coupled with the support structure; and

an integrated circuit to be tested that is disposed on and coupled with the support structure, the integrated circuit including:

a test controller;

a logic unit controller;

a single test buscoupled between the test controller and the logic unit controller;

a plurality of design for test features coupled to the logic unit controller; and

a logic unit coupled to the logic unit controller and to the design for test features,

wherein the test controller is to provide a global control signal as a packet including a plurality of different types of instruction signals to the logic unit controller over the single test bus, wherein the logic unit controller is to receive the packet and provide a plurality of different types of instruction signals to a design for test feature.

38. (New) The platform of claim 37, wherein the different types of instruction signals include a shift signal and a load signal.

39. (New) The platform of claim 37, wherein the test controller has an instruction register and a test access port finite state machine (TAP FSM), and wherein the test controller is to provide a subset of all states of the TAP FSM to the logic unit controller over the single test bus.

40. (New) The platform of claim 37, wherein the packet travels as a single speed critical global control signal, and wherein the plurality of different types of instruction signals provided to the design for test feature are not speed critical.

41. (New) The platform of claim 37, wherein the logic unit controller comprises a deskew controller.

42. (New) The platform of claim 37, wherein the packet is provided based at least in part on a clock other than a core clock of the integrated circuit.

43. (New) The platform of claim 37, wherein the single test bus comprises n number of lines such that

$$n = a + \log_2 i$$

where a is the number of ancillary transmission bits, and where $\log_2 i$ is the number of instruction bits.

44. (New) A method comprising:

generating a test information packet in a test controller of an integrated circuit;

transmitting the test information packet to a logic unit controller of the integrated circuit over a single test bus coupled between the test controller and the logic unit controller;

processing the test information packet within the at least one logic unit controller to generate a local shift signal and a local load signal; and

transmitting the local shift signal and the local load signal to a design-for-test-feature.

45. (New) The method of claim 44, wherein said transmitting the test information packet comprises transmitting the test information packet over n number of lines such that

$$n = a + \log_2 i$$

where a is a number of ancillary transmission bits, and where $\log_2 i$ is a number of instruction bits.

46. (New) The method of claim 44, wherein a shift signal and a load signal are transmitted in a single packet from the test controller to the at least one logic unit controller on the single test bus.

47. (New) The method of claim 44, wherein the test information packet is a single speed critical signal, and wherein the local shift signal and the local load signal are not speed critical signals.